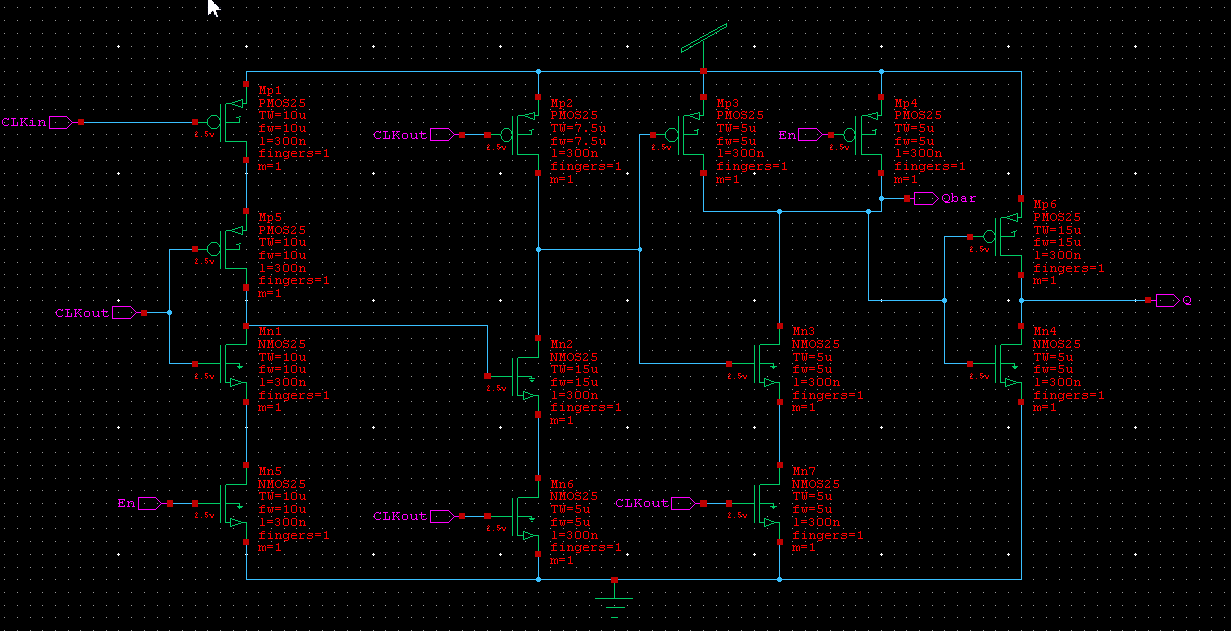
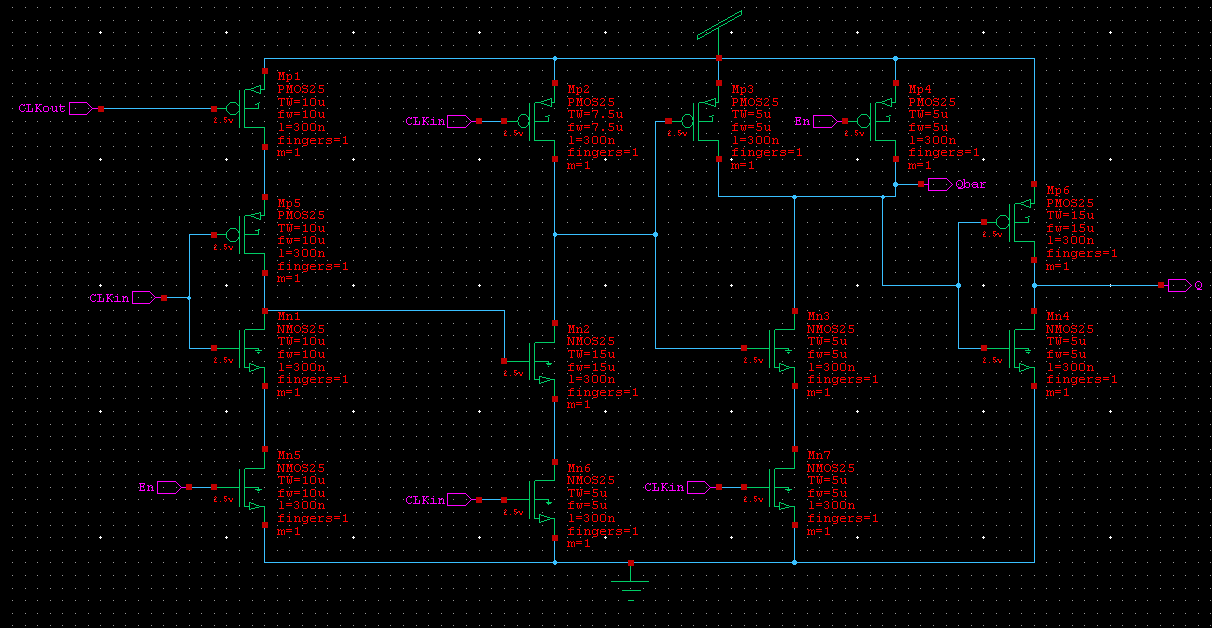
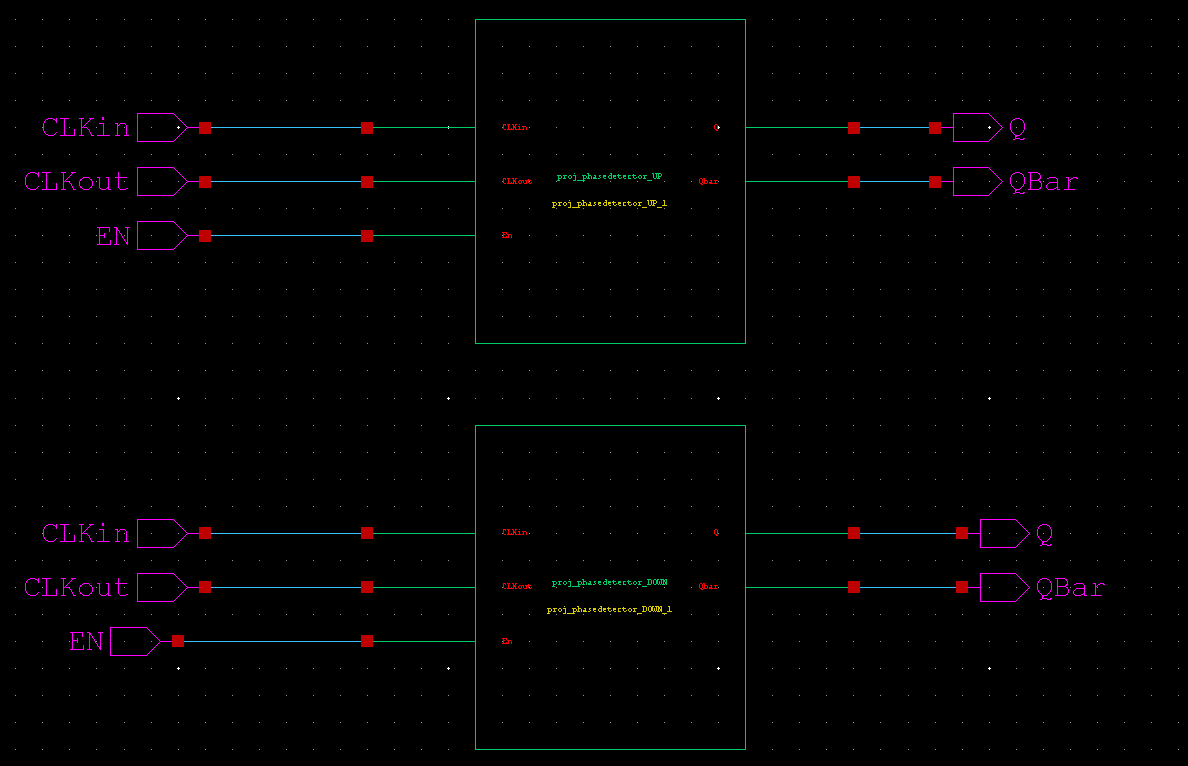
1. Phase detector up :



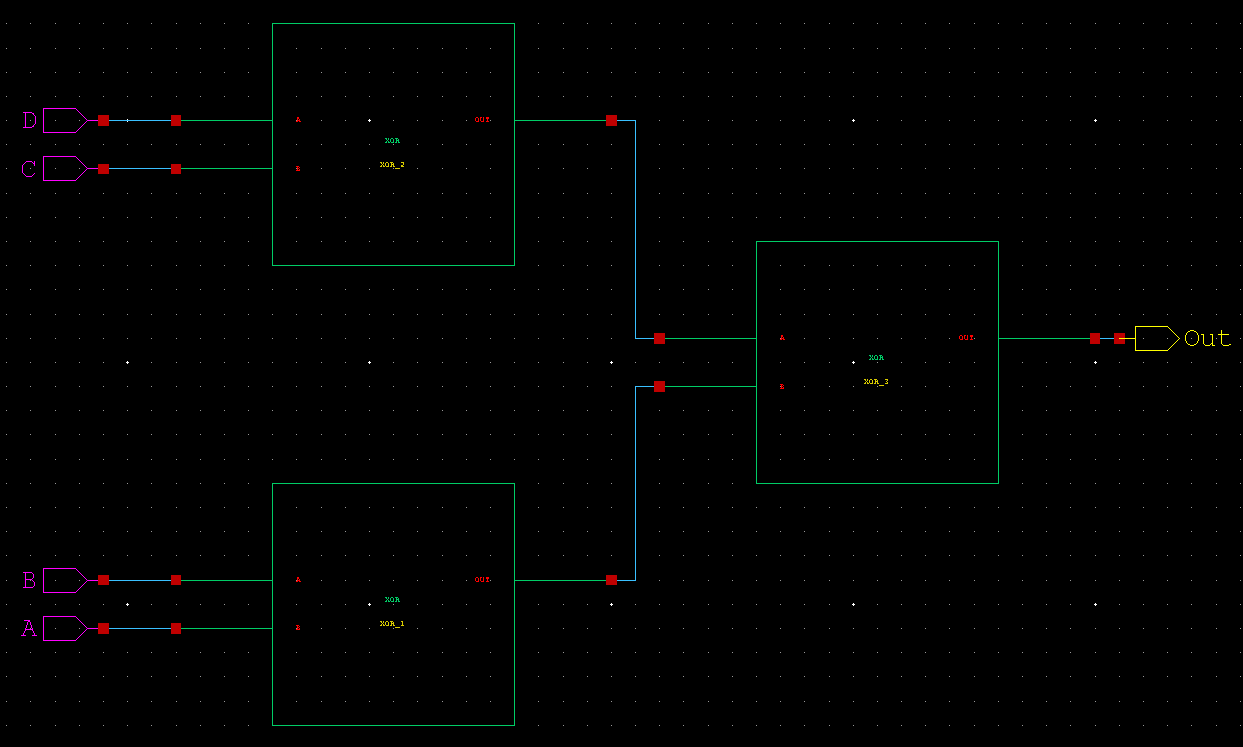
Phase detector down:



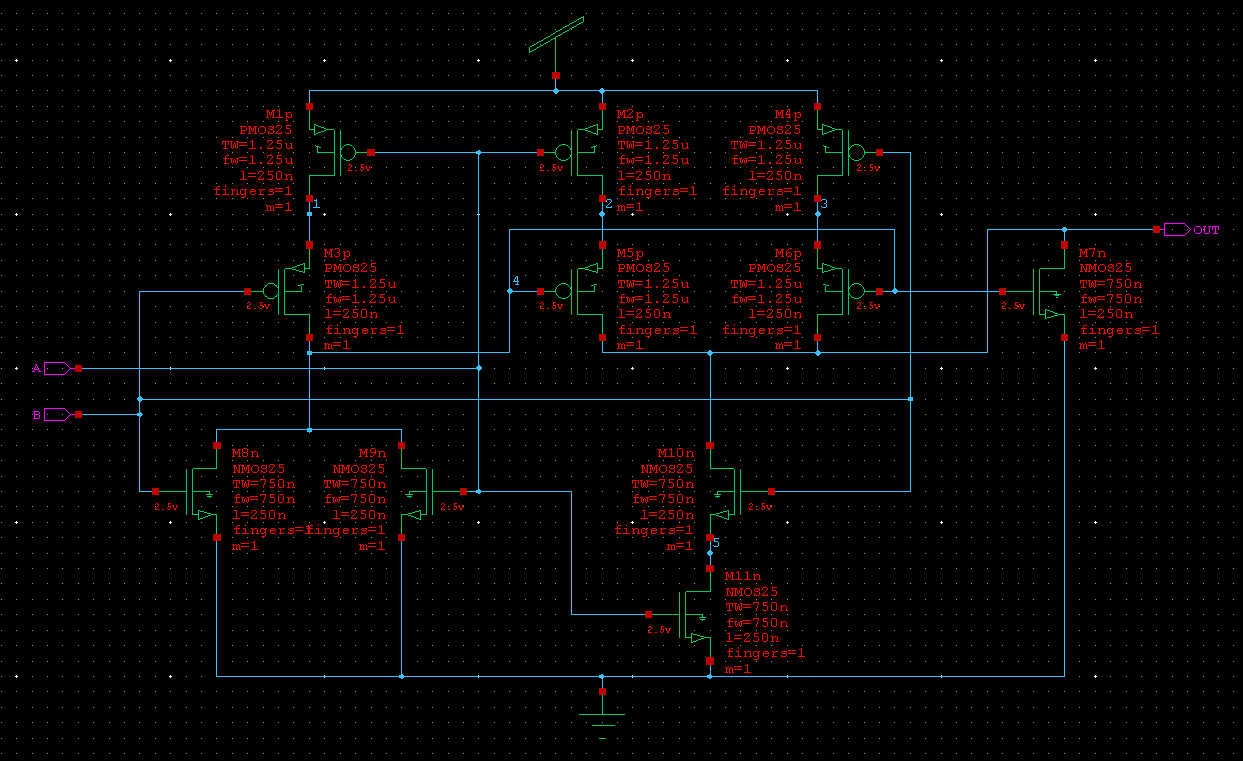
Phase detector combined :



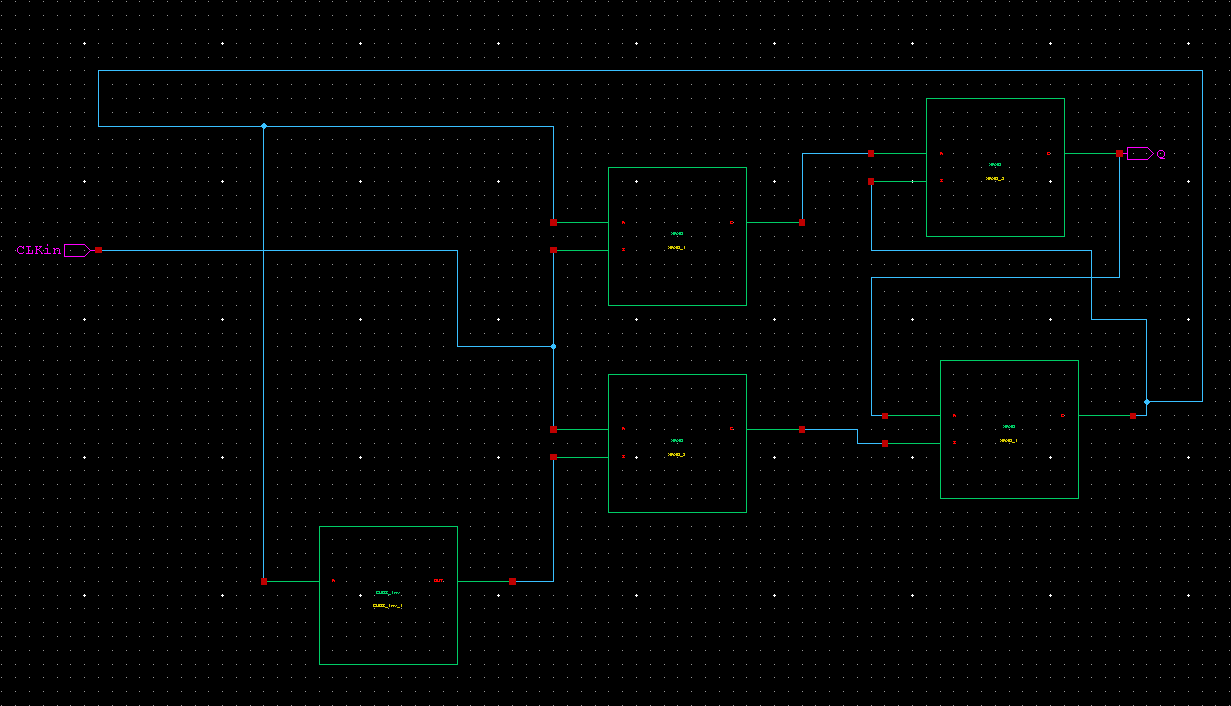
1. Edge combiner:



XOR Gate

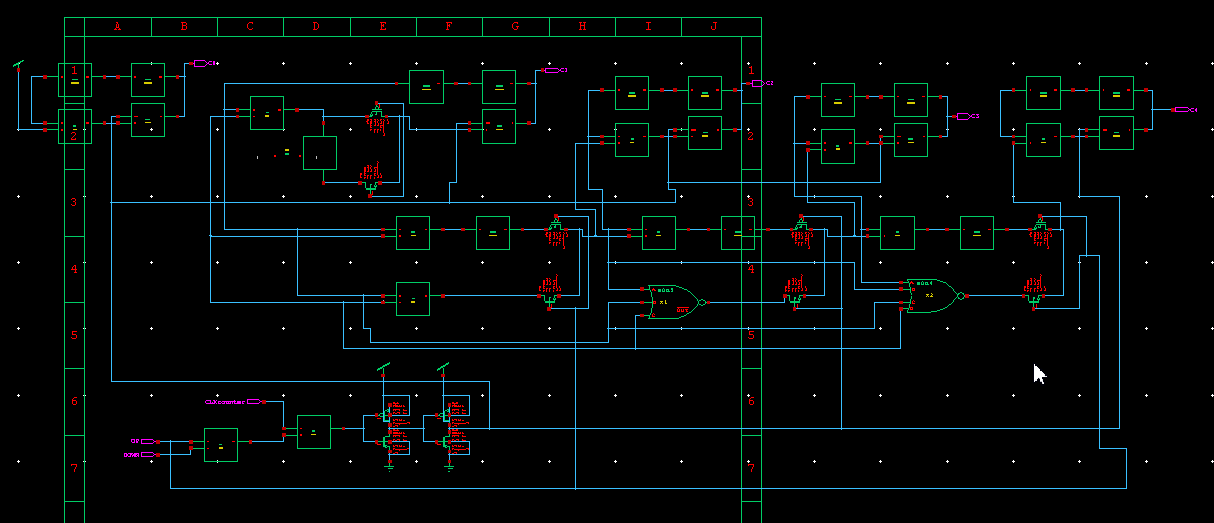


1. Divide by 2 counter

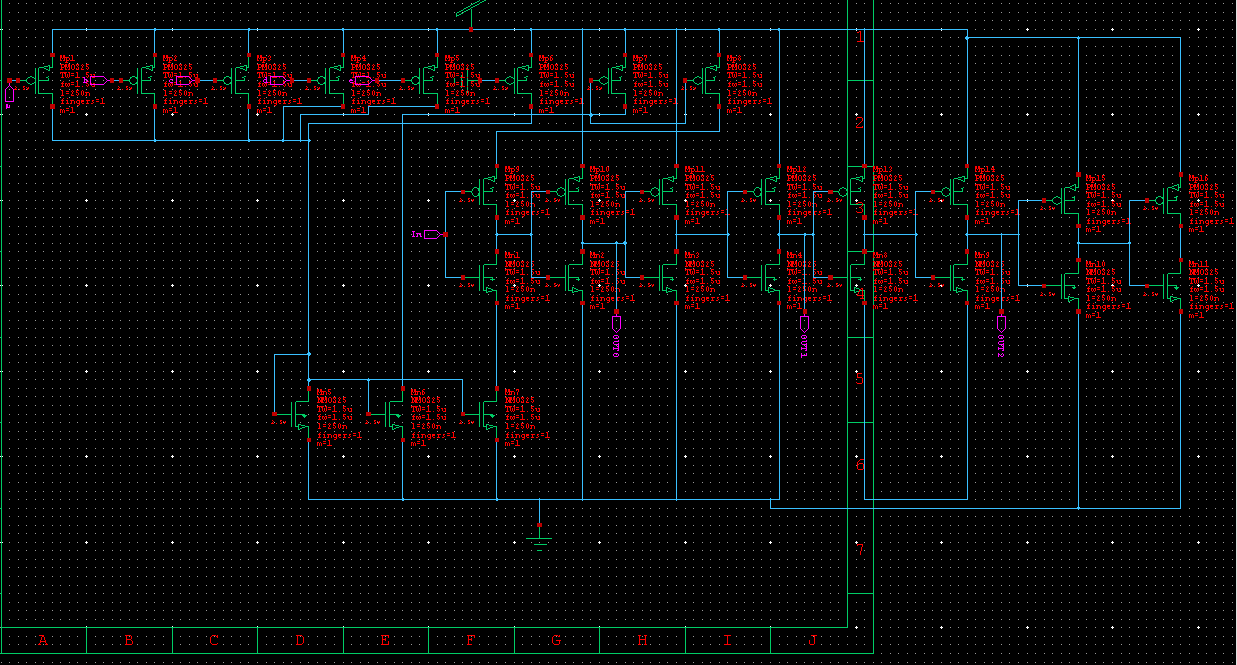


Uses cmoc inverter and nand gate

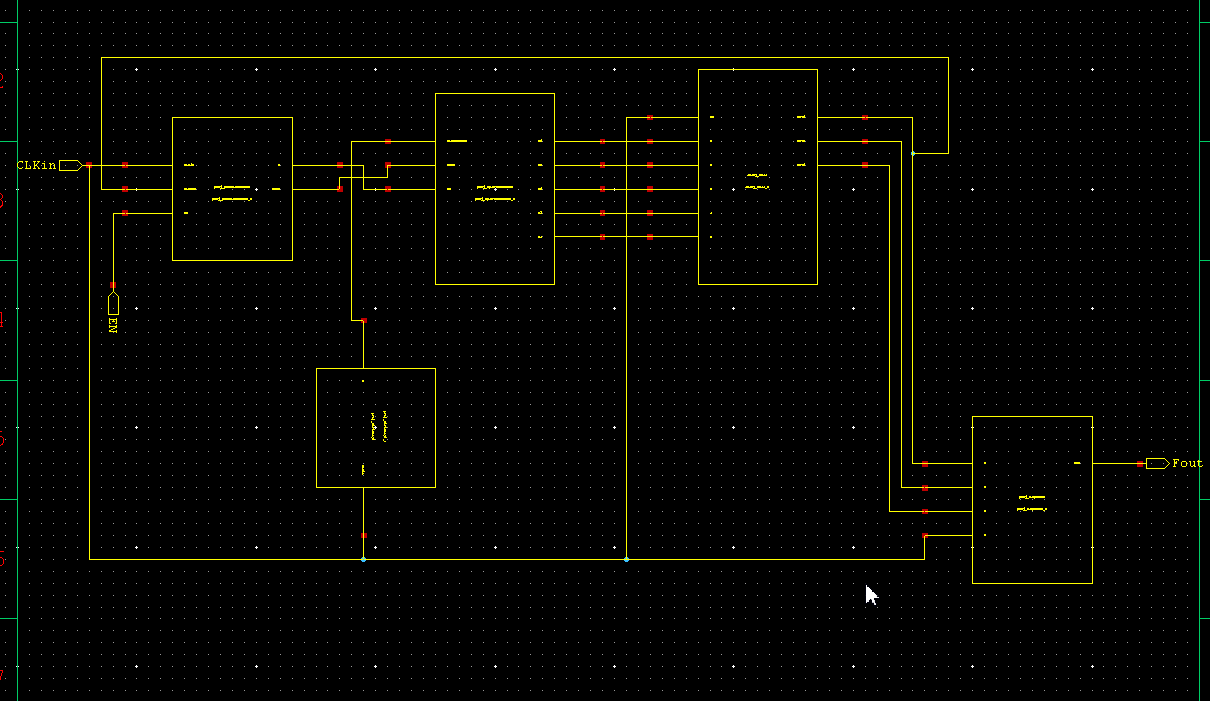
1. 5 bit updown counter



1. Delay cell



1. Overall circuit



Testbench

